HIGH-PERFORMANCE LAMINATE FOR INTEGRATED CIRCUIT INTERCONNECTION

FIELD OF THE INVENTION

The present invention relates generally to the interconnection of integrated circuits and, more particularly, to the substrates on which the integrated circuits are mounted, and even more particularly to laminate combination build-ups for such substrates, and even more particularly to layers comprising large areas of metal as typically used for ground and power planes in such build-ups.

BACKGROUND OF THE INVENTION

Printed circuit boards and substrates used for the interconnection and packaging of integrated circuit chips are typically constructed by superimposing and laminating together thin layers of insulating and conducting materials. Common construction techniques involve a high temperature lamination cycle during which the bonding of the layers to each other occurs. The resulting bonded construct is typically referred to as a laminate.

Usually at least one of the layers of the laminate is a sheet of metal with interspersed openings. Depending upon its intended purpose, the metal can serve as either a ground plane or a power plane. In addition to providing low impedance access to ground and power potentials at a relatively constant potential across the extent of the construct, these metalized planes also provide an important shielding function. Signals from metal traces on a signal layer on one side of one of the metalized planes can be shielded from signals originating from metal traces on a signal layer on the opposite side of the metalized plane. This shielding is, however, somewhat imperfect as will be explained in the following.

During the high temperature lamination process, the organic materials used in the layers create gasses. If these gasses are not allowed to exit the laminate, the resulting voids in the laminate can result in a low bonding strength and create other problems. In order to provide a path for these gases to escape, it is necessary to create a series of openings in metalized planes across the extent of the laminate. The required size and proximity of the openings and overall percent of the open areas is processing dependent. Unfortunately, these openings provide a path for coupling signals from one side of the plane to traces on the other. The resulting cross-talk is especially acute for traces that pass over the openings. Thus, solving one problem, the creation of gasses in the laminate during lamination, creates another, cross-talk between signal layers on opposite sides of the metalized plane. The higher the frequency, the greater the cross-talk problem. Since modern electronic devices are typically being driven to higher and higher frequencies, the cross-talk problem is becoming more and more of a problem.

Thus there is a need for techniques to reduce the cross-talk between two signal layers on opposite sides of a metalized ground or power layer in a laminate used in printed circuit boards and substrates intended for the interconnection and packaging of integrated circuit chips.

SUMMARY OF THE INVENTION

In accordance with aspects of the present invention, high-performance laminates for interconnecting integrated circuits are disclosed which eliminate or substantially reduce the disadvantages associated with prior interconnection techniques.

In a representative embodiment of the present invention, an interconnecting laminate includes a signal layer overlaying a conducting power/ground layer and separated by a dielectric layer of specified thickness. The signal layer includes conducting traces, and the power/ground layer is primarily a sheet of conducting material with interspersed open areas. The open areas are an essential part of the fabrication process and provide the means by which dielectric layer gasses created during fabrication can escape. In the representative embodiment, the open areas required in the power/ground layer are displaced such that none of the openings is overlain by the signal layer. Additional signal layers are included in other embodiments.

Technical advantages of the embodiments disclosed include increased speed as distributed resistance and inductance in the conducting paths are reduced. The path of conduction followed in the power/ground layer is shorter than in earlier solutions. In addition, cross-talk between two closely spaced signal lines is minimized by shielding each of their signal paths from the other. Shielding is effected via placement of the signal layers on opposite sides of the power/ground layer, and by displacement of open areas such that the open areas do not overlay the conduction paths on the signal layers.

Other aspects and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings provide visual representations which will be used to more fully describe the invention and can be used by those skilled in the art to better understand it and its inherent advantages. In these drawings, like reference numerals identify corresponding elements and:

Figure 1 is a drawing of a side view of an integrated circuit package as described in various representative embodiments of the present patent document.

Figure 2 is a drawing of a cross-sectional view of a segment of the integrated circuit package as described in various representative embodiments of the present patent document.

Figure 3 is a drawing of a power/ground layer as described in various representative embodiments of the present patent document.

Figure 4 is a drawing of overlaid layers as described in various representative embodiments of the present patent document.

Figure 5 is another drawing of power/ground layer as described in various representative embodiments of the present patent document.

Figure 6 is another drawing of the cross-section of the integrated circuit package as described in various representative embodiments of the present patent document.

Figure 7 is yet another drawing of the power/ground layer as described in various representative embodiments of the present patent document.

Figure 8 is another drawing of overlaid layers as described in various representative embodiments of the present patent document.

Figure 9 is a drawing of a topside view of overlaid layers as described in various representative embodiments of the present patent document.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

As shown in the drawings for purposes of illustration, the present patent document relates to a novel method for constructing high-performance laminate interconnections for integrated circuit interconnection. Previous methods for such constructions have relied upon metalized layers which act as power/ground planes with uniformly spaced open areas to permit the escape of gasses generated during lamination. The required size of the openings and percent open areas is processing dependent. Metal traces from signal layers typically cross these open areas creating cross-talk to signal layers on the opposite side of the power/ground layer.

In the following detailed description and in the several figures of the drawings, like elements are identified with like reference numerals.

Figure 1 is a drawing of a side view of an integrated circuit package **100** as described in various representative embodiments of the present patent document. In figure 1, an integrated circuit **105**, also referred to herein as an integrated circuit chip **105** and which in this example is a flip-chip **105**, is mounted to a ball grid array substrate **107** via solder bumps **125**. Connection from the integrated circuit package **100** is made via ball grid array pins **115**, also referred to herein as package pins **115**. Items shown in the drawings are for illustrative purposes. As such, these items are not drawn to the relative proportions to which they would be constructed in a practical application.

Figure 2 is a drawing of a cross-sectional view of a segment of the integrated circuit package **100** as described in various representative embodiments of the present patent document. In a first example, as shown in figure 2, the integrated circuit **105** is mounted to an interconnecting laminate **110**. In this example, the integrated circuit chip **105** is flip-chip **105** wherein solder bumps **125** fabricated onto metalized pads on the chip **105** are used to make electrical connection as well as to mount the chip **105** to the interconnecting laminate substrate **110**.

In the example of figure 2, the interconnecting laminate **110** comprises a first signal layer **130**, also referred to herein as a third layer **130**, a first insulating layer **135**, also referred to herein as a second layer **135**, a power/ground layer **140**, also referred to

herein as a first layer **140**, a second insulating layer **145**, also referred to herein as a fourth layer **145**, and a second signal layer **150**, also referred to herein as a fifth layer **150**.

These top layers rest on a core **175** and on the opposite side of the core **175** there are additional laminate layers **195**, which are similar in character and construction to the top layers.

The solder bumps **125** are soldered to pads **185** on the surface of the laminate substrate **110**. The pads **185** then connect to electrically conducting traces **155** on the first signal layer **130**. The combination of traces **155** and vias **160** provides a path for the signal to traverse through the layers **130,135,140,145,150,175,195** to make contact with the package pins **115**. It will be understood by one of average skill in the art that other applications are possible, as for example, multiple chips **105** mounted in the same package **100** and multiple integrated circuit packages **100** mounted on a printed circuit board wherein the printed circuit board performs a similar interconnection function as shown in figure 2. It will also be understood by one of average skill in the art that other layer stack configurations and constructs with multiple signal, insulating, ground and power layers present in practical applications are not shown in figure 2. These items have not been shown for clarity of illustration.

The power/ground layer **140** comprises an electrically conducting area **165** and open areas **170**. In this example, one of the open areas **170** is located directly over trace **155** on second signal layer **150** and directly under trace **155** located on first signal layer **130** resulting in a relatively strong cross-talk between the two traces **155**.

Figure 3 is a drawing of power/ground layer **140** as described in various representative embodiments of the present patent document. For clarity of illustration, figure 3 shows only a part of the power/ground layer **140** of the laminate **110** of the example of figure 2. As previously stated, the power/ground layer **140** comprises the electrically conducting area **165** and multiple open areas **170**. The open areas each have a centroid **171**, only one of which is shown in figure 3 for clarity of illustration. The open areas **170** in a typical application have a repeating size, a repeating shape, and a repeating orientation with respect to a Cartesian coordinate system **178**, and the open areas **170** are interspersed inside an outer perimeter **180** of the electrically conducting

area **165**. Also shown is the opening for via **160** in the power/ground layer **140**.

Figure 4 is a drawing of overlaid layers as described in various representative embodiments of the present patent document. Shown in figure 4 is the power/ground layer **140** of the example of figure 3 which is only a part of the example of figure 2. Also, shown overlaying the power/ground layer **140** is solder bump **125** bonded to solder bump pad **185** attached to trace **155** on the first signal layer **130**. The opposite end of trace **155** is connected to a capture pad **190**, also referred to as a land **190**, that connects to the via **160** which is then connected to a series of additional traces and vias to provide electrical connection to one of the package pins **115**. In figure 4, as well as figure 2, the trace **155** overlays several open areas **170**.

Figure 5 is another drawing of power/ground layer **140** as described in various representative embodiments of the present patent document. In figure 5, an effective return path **156** on the power/ground layer **140** for the signal carried by the trace **155** on the first signal layer **130** is shown. Note that this effective return path **156** is longer than it would be if the trace **155** did not overlay the open areas **170**.

Figure 6 is another drawing of the cross-section of the integrated circuit package **100** as described in various representative embodiments of the present patent document. In the preferred embodiment of figure 6, the interconnecting laminate **110** comprises the first signal layer **130**, the first insulating layer **135**, the power/ground layer **140**, the second insulating layer **145**, and the second signal layer **150**. These top layers rest on the core **175**. On the opposite side of the core there are additional laminate layers **195**.

The solder bumps **125** are soldered to pads **185** on the surface of the laminate substrate **110**. The pads **185** then connect to electrically conducting traces **155** on the first signal layer **130**. The combination of traces **155** and vias **160** provides a path for the signal to traverse through the layers **130,135,140,145,150,175,195** to make contact with the package pins **115**. Again, it will be understood by one of average skill in the art that other layers and constructs which would be present in practical applications are not shown in figure 6. These items have not been shown for clarity of illustration.

The power/ground layer **140** comprises the electrically conducting area **165** and open areas **170**. In this second example, open areas **170** are located so that they do not

lie directly over trace **155** on second signal layer **150**, and open areas **170** are located so that they do not lie directly under trace **155** located on first signal layer **130**. The construct of figure 6 results in very good shielding between the two traces **155** with associated relatively reduced cross-talk.

Figure 7 is yet another drawing of the power/ground layer **140** as described in various representative embodiments of the present patent document. For clarity of illustration, figure 7 shows only a part of the power/ground layer **140** of the laminate **110** of the example of figure 6. As previously stated, the power/ground layer **140** comprises the electrically conducting area **165** and multiple open areas **170**. The open areas **170** generally have a repeating size, a repeating shape, and a repeating orientation with respect to the Cartesian coordinate system **178**, and the open areas **170** are interspersed inside the outer perimeter **180** of the electrically conducting area **165.** Also shown is the opening for via **160** in the power/ground layer **140**. Many different patterns may be created when designing and fabricating the open areas **170** to achieve the percent area coverage needed for the effective release of the gases from the laminate substrate **110**. These open areas **170** may be random in both shape, size, and/or placement, or they may be repeating in shape and/or size with or without being regular in their placement. The percentage of the power/ground layer **140** consumed by the open areas **170** will be preferably greater than or equal to 10% and less than or equal to 30%.

Figure 8 is another drawing of overlaid layers as described in various representative embodiments of the present patent document. Shown in figure 8 is the power/ground layer **140** of the example of figure 7 which is only a part of the example of figure 6. Also, shown overlaying the power/ground layer **140** is solder bump **125** bonded to solder bump pad **185** attached to trace **155** on the first signal layer **130**. The opposite end of trace **155** connected to capture pad **190** that connects to the via **160** which is then connected to a series of additional traces and vias to provide electrical connection to one of the package pins **115**. Note that in figure 8, as well as figure 6, the trace **155** on first signal layer **130** overlays only electrically conducting area **165** on the power/ground layer **140**. As stated above, the construct of figures 5, 6, and 7 results in very good shielding between the two traces **155** with associated relatively reduced cross-

talk.

In addition, the effective inductance and resistance of traces for the first example of figures 2 and 4 is greater than that for the traces **155** and power/ground layer **140** return path of the second example of figures 6 and 8 which would result in a greater delay time and thus speed of the packaged integrated circuit **105**.

Figure 9 is a drawing of a topside view of overlaid layers as described in various representative embodiments of the present patent document. In figure 9, multiple traces **155** on first and second signal layers **130,150** originating from closely spaced end points, as for example neighbor solder bumps **125**, and terminating on more widely spaced end points, as for example, package pins **115**, would form a radial appearing pattern on both signal layers **130,150** and on power/ground layer **140**.

A primary advantage of the embodiment as described in the present patent document over prior techniques for the construction of power/ground layers **140** in interconnecting laminate **110** for integrated circuit chips **105** is the reduction in cross-talk between signal layers **130,150** lying on opposite sides of the power/ground layer **140**. A further advantage is the reduction in the effective resistance and inductance of the interconnecting traces **155**.

While the present invention has been described in detail in relation to preferred embodiments thereof, the described embodiments have been presented by way of example and not by way of limitation. It will be understood by those of ordinary skill in the art that various changes may be made in the form and details of the described embodiments resulting in equivalent embodiments that remain within the scope of the appended claims.